REMARKS

Claims 1, 4-6, 8, 9, 13-17, 21, 26, 28-33, 38, 39, and 41-43 are amended. Claims 2, 3, 11, 12, 35, 36, 47, and 50-93 are cancelled, without prejudice to their underlying subject matter. Claims 23, 30, 33, and 44 have been withdrawn from consideration by the Examiner as allegedly directed to a non-elected species. Claims 1-34, 37-46, 48, and 49 are pending.

Claims 1-4, 6-10, 13, 14, 21, 22, 24-29, 31, 38, 39, 41-43, 45, 50, 51, 85, 86, 88, and 89 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,166,405 ("Kuriyama et al.") in view of U.S. Patent 5,780,902 ("Komuro"). Applicant respectfully traverses this rejection.

Applicant renews its argument that, as of the filing date, there would have been no motivation to combine the cited references for the purpose of the present obviousness objection. There is simply nothing in either reference to suggest the desirability or utility of utilizing the transistor structure disclosed in Komuro with a photosensor structure like that disclosed by Kuriyama et al. There is no motivation evidenced in the cited references themselves for selectively combining their teachings in the manner expressed in the Office Action, nor would there have been any practical reason to deviate from the disclosure of the primary reference; i.e., "no objective reason." Absent the impermissible use of hindsight utilizing the present application as a roadmap, Kuriyama et al. would not have been combined with Komuro to achieve the recited subject matter.

Moreover, claim 1, as amended, defines a CMOS imager and recites "a photoconversion device" and "a transfer transistor, said transfer transistor comprising a transfer gate with a first side and a second side opposite said first side, said transfer

gate being associated with said photoconversion device at said first side of said transfer gate" and "a reset transistor at said second side of said transfer gate, said reset transistor comprising a reset gate" and "a floating diffusion region at said second side of said transfer gate, between said transfer gate and said reset gate, said floating diffusion region comprising an active area extension region at said second side of said transfer gate and a halo implant region below said active area extension region, wherein said floating diffusion region is closer to said reset gate than to said transfer gate." Such a device is not taught or suggested by Kuriyama et al. and Komuro.

Kuriyama et al. and Komuro, even if properly combined, which they are not, do not teach or suggest "a floating diffusion region at said second side of said transfer gate, between said transfer gate and said reset gate, said floating diffusion region comprising an active area extension region at said second side of said transfer gate and a halo implant region below said active area extension region, wherein said floating diffusion region is closer to said reset gate than to said transfer gate" in combination with the other recited features. The combined references do not teach or suggest any relationship between a floating diffusion region and a transfer gate and a reset gate, much less that the floating diffusion region is closer to one than the other. For at least this reason, independent claim 1 and each dependent claim is patentable over Kuriyama et al. and Komuro.

Additionally, Kuriyama et al. and Komuro do not teach or suggest "said transfer transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant" as recited by claim 4. The Office Action indicates that a halo implant, as recited in claim 1, is interpreted as the same as the threshold voltage implant as recited at claim 4. This is an incorrect reading of the claim. These two regions are not the same; these separate and distinct limitations must be

interpreted as different features of the claimed device. The halo implant of claim 1 is located to be associated with the floating diffusion region between the transistor gates; it is positioned so that it can prevent punch through (Specification ¶ 0033, 0045). The threshold voltage implant of claim 4 is located at the transfer transistor's channel region; it is positioned to tune the switching of the transistor, compensate for the asymmetrical active area extension region, prevent punch through and prevent charge leakage (Specification ¶¶ 0026, 0042, 0044). The combined references do not teach or suggest these features. In addition to the reasons set forth above for the patentability of claim 1, claim 4 is patentable for this reason as well.

Additionally, Kuriyama et al. and Komuro do not teach or suggest "said active area extension region and said halo implant region are laterally spaced away from the transfer gate by a portion of a substrate supporting said first transistor and including said active area extension region," as recited by claim 8. Neither reference teaches or suggests that a portion of the substrate laterally spaces apart the transfer gate and the active area extension region (and halo implant region), as claimed. Both references show their respective LDD regions as being immediately below and adjacent the transistor gates (Fig. 1 of Kuriyama et al. and Fig. 5c of Komuro). Even if there is a vertical spacing between these regions and the transistor gate, this is not a lateral spacing. There is no lateral portion of the substrate separating the transistor gates of the references from their LDD region or pocket (designated a halo by the Office Action) region. In addition to the reasons set forth above for the patentability of claim 1, claim 8 is patentable for this reason as well.

Additionally, neither Kuriyama et al. nor Komuro teaches or suggests "at least one of said reset transistor and said source follower transistor have a single active area extension region," as recited by claim 10. If it were obvious to include another

transistor, in addition to the transfer transistor, having a single active area extension in an imager pixel, Kuriyama et al., the reference cited as disclosing use of a single LDD opposite a photodiode, would have at least hinted that such were possible or desirable. Kuriyama et al. (and Komuro) does not teach or suggest this. In addition to the reasons set forth above for the patentability of claim 1, claim 10 is patentable for this reason as well.

For at least the above reasoning, independent claim 1 and dependent claims 2-4, 6-10, 13, and 14 are patentable over the references. The 35 U.S.C. § 103(a) rejection of claims 1-4, 6-10, 13, and 14 is respectfully requested to be withdrawn.

Claim 21, as amended, defines a pixel sensor cell and recites "a semiconductor substrate" and "a reset transistor over said substrate" and "a photosensor in electrical communication with said reset transistor, said photosensor being within said substrate on a first side of said reset transistor" and "a single active area extension region in said substrate adjacent to said reset transistor, said single active area extension region being on a side of said reset transistor which is opposite to said first side" and "a halo implant region in said substrate below said single active area extension region" and "an n-type layer at the surface of said substrate and over said single active area extension region." Such a device is not taught or suggested by Kuriyama et al. and Komuro.

The combination of Kuriyama et al. and Komuro, even though improperly combined, does not teach or suggest "an n-type layer at the surface of said substrate and over said single active area extension region" in combination with the other recited features. No n-type layer in such a configuration is taught or suggested by the references. For at least this reason, the subject matter of independent claim 21 and its dependent claims is patentable over the references.

Also, as discussed above in relation to the patentability of claim 4, Kuriyama et al. and Komuro do not teach or suggest the threshold voltage adjustment implant recited by claim 22 as combined with the other features of independent claim 21. Therefore, claim 22 is patentable for this reason as well.

Since independent claim 21 is patentable over Kuriyama et al. and Komuro, so are dependent claims 22, 24, and 25. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 21, 22, 24, and 25 is respectfully requested to be withdrawn.

Claim 26, as amended, defines an image sensor and recites "a semiconductor substrate" and "a transfer gate over said substrate" and "a reset gate over said substrate, wherein said transfer gate has a gate length greater than that of said reset transistor" and "a floating diffusion region in said substrate and between said transfer gate and said reset gate, said floating diffusion region being closer to said reset gate than to said transfer transistor gate" and "a single active area extension region in said substrate adjacent to said transfer gate and said floating diffusion region" and "a halo implant region in said substrate below said single active area extension region" and "an n-type surface layer over said floating diffusion region and said single active area extension region" and "a threshold voltage implant in said substrate below said transfer gate" and "a photodiode adjacent said transfer gate at a side opposite said active area extension region and said floating diffusion region." Such a device is not taught or suggested by Kuriyama et al. and Komuro.

As discussed above in relation to the patentability of claim 1 over these references, Kuriyama et al. and Komuro do not teach or suggest "a floating diffusion region in said substrate and between said transfer gate and said reset gate, said floating diffusion region being closer to said reset gate than to said transfer transistor gate," as

recited by the claim. Additionally, as discussed above in relation to the patentability of claim 21, the references also do not teach or suggest "an n-type surface layer over said floating diffusion region and said single active area extension region," as also recited by the claim. Further, Kuriyama et al. and Komuro, as discussed above in relation to the patentability of claims 4 and 22, do not teach or suggest "a halo implant region in said substrate below said single active area extension region" and "a threshold voltage implant in said substrate below said transfer gate," as recited by the claim. For each of these reasons, independent claim 26 and the depending claims are patentable over Kuriyama et al. and Komuro.

Additionally, as discussed above in relation to the patentability of claim 8, neither Kuriyama et al. nor Komuro teaches or suggests "said floating diffusion region and said single active area extension region are laterally separated from said transfer gate in a direction toward said reset gate by a portion of said substrate," as recited by claim 28. This provides reasoning in addition to that discussed above in relation to independent claim 26 for the patentability of claim 28 over the cited references.

Additionally, as discussed above in relation to the patentability of claim 10, neither Kuriyama et al. nor Komuro teaches or suggests "at least one of said reset gate, said source follower gate, and said row select gate are associated with a second single active area extension region," as recited by claim 30. This provides reasoning in addition to that discussed above in relation to independent claim 26 for the patentability of claim 30 over the cited references.

Additionally, neither Kuriyama et al. nor Komuro teaches or suggests "said transfer gate has a gate length greater than that of said source follower gate and said row select gate," as recited by claim 31. This provides reasoning in addition to that

discussed above in relation to independent claim 26 for the patentability of claim 31 over the cited references.

Claim 38, as amended, defines an integrated circuit and recites "a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region on a side of said transistor opposite from said photodiode, a halo implant below said single active area extension region, an n-type layer over said single active area extension region, and a threshold voltage implant below said transistor." Kuriyama et al. and Komuro do not teach or suggest such a device.

As discussed above in relation to the patentability of claims 4, 22, and 26, Kuriyama et al. and Komuro do not teach or suggest "a halo implant below said single active area extension region" and "a threshold voltage implant below said transistor." Additionally, the combined references do not teach or suggest "an n-type layer over said single active area extension region," as discussed above in relation to the patentability of claims 21 and 26. Therefore, for at least the same reasons as set forth above for the patentability of claims 4, 21, 22, and 26, independent claim 38, as well as each depending claim, is likewise patentable over Kuriyama et al. and Komuro.

Additionally, as discussed above in relation to the patentability of claims 8 and 28, neither Kuriyama et al. nor Komuro teaches or suggests "said active area extension region and said floating diffusion region are laterally spaced away from a gate of said transistor by a portion of a substrate supporting said transistor," as recited by claim 41. This provides reasoning in addition to that discussed above in relation to independent claim 38 for the patentability of claim 41 over the cited references.

For the reasons set forth above, independent claim 38 and dependent claims 39, 41-43 and 45 are patentable over Kuriyama et al. and Komuro. Applicant

respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 38, 39, 41-43, and 45 be withdrawn.

Claims 15, 16, and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuriyama et al. in view of Komuro and U.S. Patent 6,794,215 ("Park et al."). Applicant respectfully traverses this rejection.

Claim 15, as amended, defines a pixel sensor cell and recites "a semiconductor substrate" and "a transfer transistor over said substrate, said transfer transistor having a single active area extension region located on a first side of said transfer transistor" and "a photosensor in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side" and "a reset transistor gate over said substrate and spaced apart from said transfer transistor" and "a floating diffusion region on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region being in electrical communication with said active area extension region and comprising a halo implant region below said single active area extension region and an n-type doped region at the surface of said substrate and spanning said floating diffusion region and said single active area extension region." Such a device is not taught or suggested by Kuriyama et al., Komuro and Park et al.

Park et al. is cited in the Office Action for its alleged disclosure of a reset transistor with an transfer transistor. Nevertheless, Kuriyama et al., Komuro and Park et al. fail to teach or suggest "a floating diffusion region on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region being in electrical communication with said active area extension region and comprising a halo implant region below said single active area extension region and an n-type doped region at the surface of said substrate and spanning said floating diffusion region and

said single active area extension region." No such configuration of floating diffusion region, active area extension region, halo implant, and n-type doped region is taught or suggested by any of the three references, individually or in combination. For this reason, independent claim 15, and each depending claim, is patentable over Kuriyama et al., Komuro, and Park et al.

Additionally, Kuriyama et al., Komuro, and Park et al. fail to teach or suggest "said transfer transistor has a threshold voltage adjustment implant in said substrate below a gate of said transfer transistor," as recited by claim 16. This lack of teaching or suggestion in Kuriyama et al. and Komuro has been discussed above in relation to the patentability of claims 4, 22, 26, and 38 over these references; Park et al. cannot supplement Kuriyama et al. and Komuro for such a disclosure and therefore the trio combined would not have rendered the claimed subject matter obvious. For this reason, also, claim 16 is patentable over Kuriyama et al., Komuro, and Park et al.

Additionally, Kuriyama et al, Komuro, and Park et al. fail to teach or suggest the pixel sensor cell configuration where the reset transistor "comprises two active area extension regions as lightly doped drains," as recited by claim 18. No combination of transfer transistor have one active area extension region and a reset transistor having two is taught or suggested by the references. For this reason, also, claim 18 is patentable over Kuriyama et al., Komuro, and Park et al.

Additionally, Kuriyama et al, Komuro, and Park et al. fail to teach or suggest the pixel sensor cell configuration where the reset transistor "comprises a single active area extension region on a side opposite said floating diffusion region," as recited by claim 19. No combination of transfer transistor and reset transistor, each having only one active area extension region, much less the specific locations of such active area extension regions (opposite the photosensor for the transfer transistor and opposite the

floating diffusion region for the reset transistor) is taught or suggested by the references. For this reason, also, claim 19 is patentable over Kuriyama et al., Komuro, and Park et al.

For at least each of the reasons set forth above, independent claim 15 and dependent claims 16 and 18-20 are patentable over Kuriyama et al., Komuro, and Park et al. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn.

Claims 1, 5, 15, 17, 32, 34, 37, 38, 40, 46,48-52, 85, and 87 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,730,899 ("Stevens et al.") in view of Kuriyama et al. and Komuro. Applicant respectfully traverses this rejection. Although the patent number of the "Stevens" reference cited in the Office Action is not indicated, Applicant assumes for the purposes of providing a complete response that the Office Action is referring to the Stevens et al. patent already made of record in the prior office action.

Claim 1 has been discussed at length above as being patentable over Kuriyama et al. and Komuro. Stevens et al. is cited in the Office Action for its alleged disclosure of a basic CMOS pixel cell and for its alleged disclosure of varyied gate length with respect to the transfer gate and other transistor gates of a pixel cell. Stevens et al., Kuriyama et al., and Komuro do not teach or suggest "a floating diffusion region at said second side of said transfer gate, between said transfer gate and said reset gate, said floating diffusion region comprising an active area extension region at said second side of said transfer gate and a halo implant region below said active area extension region, wherein said floating diffusion region is closer to said reset gate than to said transfer gate" in combination with the other features recited by independent claim 1. The combined references do not teach or suggest any relationship between a floating

diffusion region and a transfer gate and a reset gate, much less that this region is closer to one transistor gate than the other. For this reason, independent claim 1 and each dependent claim is patentable over Stevens et al., Kuriyama et al. and Komuro.

Additionally, with regard to dependent claim 5, Stevens et al., Kuriyama et al., and Komuro fail to teach or suggest "said transfer transistor has a gate length which is greater than that of all other transistors of a same pixel cell," as recited by the claim. Even if Stevens et al. does disclose that a transfer gate has a gate length increased relative to some other transistors, which Applicant contests since it is no discussed anywhere in the reference, it does not teach or suggest that the transfer transistor gate length is increased relative to "all other transistors of a same pixel cell." Based on the reasoning in the Office Action, since the (not to scale) drawing of Stevens et al. Fig. 2 shows that the transfer gate (TG) is not of increased gate length relative to the amplifier gate (100), it is not increased relative to all other transistor in the pixel. For this reasoning, also, dependent claim 5 is patentable over Stevens et al., Kuriyama et al. and Komuro.

Claim 15 has been discussed above as patentable over Kuriyama et al. and Komuro (and Park et al.); it is likewise patentable if these references are combined with Stevens et al. Kuriyama et al., Komuro, and Stevens et al. fail to teach or suggest "a floating diffusion region on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region being in electrical communication with said active area extension region and comprising a halo implant region below said single active area extension region and an n-type doped region at the surface of said substrate and spanning said floating diffusion region and said single active area extension region." No such configuration of floating diffusion region, active area extension region, halo implant, and n-type doped region is taught or suggested by any

of the three references, individually or in combination. For this reason, independent claim 15, as well as each dependent claim, is patentable over Kuriyama et al., Komuro, and Stevens et al.

Additionally, as with claim 5 discussed above, Stevens et al., Kuriyama et al., and Komuro fail to teach or suggest "said transfer transistor has a gate length which is greater than that of all other transistors of a same pixel cell," as recited by claim 17. Even if Stevens et al. does disclose that a transfer gate can have a gate length that is increased relative to other transistors, which Applicant contests for the lack of any discussion of such in the reference, it does not teach or suggest that the transfer transistor gate length is increased relative to "all other transistors of a same pixel cell." Based on the reasoning in the Office Action, since the (not to scale) drawing of Stevens et al. Fig. 2 shows that the transfer gate (TG) is not of increased gate length relative to the amplifier gate (100), it is not increased relative to all other transistor in the pixel. For this reasoning, also, dependent claim 17 is patentable over Stevens et al., Kuriyama et al. and Komuro.

For the reasons discussed above, independent claim 15 and dependent claim 17 are patentable over Stevens et al., Kuriyama et al., and Komuro. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn.

Claim 32, as amended, defines an imager device and recites "an image processor" and "a pixel array for supplying signals to said image processor, at least one pixel of said array comprising: a photoconversion device" and "a first transistor gate associated with said photoconversion device at a first side of said transistor gate, said gate having a length which is greater than that of all other transistor gates of said pixel" and "a single lightly doped drain on a second side of said transistor gate opposite said first side" and "a channel region under said transistor gate and comprising a threshold

voltage adjustment implant" and "a halo implant below said lightly doped drain." Such a device is not taught or suggested by Stevens et al., Kuriyama et al., and Komuro.

Stevens et al., Kuriyama et al. and Komuro fail to teach or suggest "a first transistor gate associated with said photoconversion device at a first side of said transistor gate, said gate having a length which is greater than that of all other transistor gates of said pixel," as recited by independent claim 32. This failing of the combined references is discussed above in relation to the patentability of claims 5 and 17. Additionally, the combined references fail to teach or suggest "a channel region under said transistor gate and comprising a threshold voltage adjustment implant" and "a halo implant below said lightly doped drain." It has been discussed above that Kuriyama et al. and Komuro fail to teach or suggest such a feature; Stevens et al. likewise fails and cannot supplement the other references in this regard. Therefore, independent claim 32, and each dependent claim, is patentable over these references.

For the above reasons, independent claim 32 and dependents claims 34 and 37 are patentable over Stevens et al., Kuriyama et al., and Komuro. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn.

Claim 38 has been discusses above as patentable over Kuriyama et al. and Komuro. These references were discussed as not teaching or suggesting "a halo implant below said single active area extension region" and "a threshold voltage implant below said transistor" and also not teaching or suggesting "an n-type layer over said single active area extension region." Stevens et al. likewise fails in this regard. Therefore, independent claim 38, and each dependent claim, is patentable over these references.

Also, as discussed above in relation to the patentability of claims 17 an 32, Stevens et al., Kuriyama et al., and Komuro fail to teach or suggest "said transistor has a gate length which is increased relative to any transistor gate length of other transistors of a same pixel," as recited by claim 40. For this reason as well, claim 40 is patentable over these references.

For the reasons set forth above, independent claim 38 and dependent claim 40 are patentable over Stevens et al., Kuriyama et al., and Komuro. The rejection of these claims under 35 U.S.C. § 103(a) over these references is respectfully requested to be withdrawn.

Claim 46 defines a pixel cell and recites "a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region and halo implant region on a opposite side of said transistor from said photodiode, said transistor also having a gate length which is increased relative to any other transistor gate length of transistors of a same pixel." This device is not taught or suggested by Stevens et al., Kuriyama et al., and Komuro.

As discussed above in relation to the patentability of claims 5, 17, 32, and 40, the combination of Stevens et al., Kuriyama et al., and Komuro fails to teach or suggest "transistor also having a gate length which is increased relative to any other transistor gate length of transistors of a same pixel." Stevens et al., cited for the purpose of its alleged disclosure of such a gate length feature, fails to teach or suggest that any of its disclosed transistor gates has a longer gate length than all the other transistors of the same pixel. For this reason, independent claim 46 and dependent claims 48 and 49 are patentable over these references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 46, 48, and 49 be withdrawn.

Applicant believes all pending claims are in immediate condition for allowance and respectfully requests a Notice of Allowance for all pending claims (1-35, 37-52, and 85-93).

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Respectfully submitted,

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